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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			EXAMINER GREEN, PHILLIP	
			ART UNIT 2823	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/566,984

Applicant(s)

CHUA ET AL.

Examiner

Phillip S. Green

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 December 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2006 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 02/02/2006.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-25 in the reply filed on December 07, 2007 is acknowledged.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4-12, 15-17, 20, 21 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (US 7037767 B2).

Re claim 1, Hirai teaches a method of making a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of:

(i) depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer; and

(Note: Column 15, lines 17-23)

(ii) optionally curing the layer deposited in step (i); (Note: Column 15, lines 30-36)

wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer. (Note: Column 15)

Re claim 2, as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) is in the range of from 0.5 to 2. (Note: Column 4)

Re claim 4, as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution. (Note: Column 3, lines 65- Column 4, line 2)

Re claim 5, as applied to claim 4 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer comprises oligomers and/or monomers for forming the insulating polymer and the material for forming the semiconductive layer comprises a semiconductive polymer and/or oligomers for forming the semiconductive polymer. (Note: Columns 4-8)

Re claim 6, as applied to claim 4 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer comprises an insulating polymer and the material for forming the semiconductive layer comprises a

semiconductive polymer and/or oligomers for forming the semiconductive polymer.

(Note: Columns 4-8)

Re claim 7, as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the semiconductive layer and the material for forming the dielectric layer comprises a diblock polymer, said polymer comprising a semiconductive block for forming the semiconductive layer and a dielectric block for forming the dielectric layer. (Note: Columns 4-8)

Re claim 8, as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the semiconductive layer comprises one or more aromatic or heteroaromatic structural units. (Note: Columns 4-8)

Re claim 9, as applied to claim 8 above, Hirai teaches all the claimed limitations including, wherein the one or more aromatic or heteroaromatic units independently are selected from the group consisting of fluorenyl, phenylene, phenylene vinylene, triarylamine, thiophenediyl, thiophene, oxadiazole and benzothiadiazole. (Note: Column 11, lines 54-64)

Re claim 10 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer comprises crosslinkable groups. (Note: Columns 4-8)

Re claim 11 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer comprises one or more units having a low cohesive-energy density. (Note: Columns 4-8)

Re claim 12 as applied to claim 11 above, Hirai teaches all the claimed limitations including, wherein the one or more units having a low cohesive-energy density are selected from the group consisting of siloxane, perfluoroalkyl, perfluoroarylene ether, perfluoroalkylene ether. (Note: Columns 4-8)

Re claim 15 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the transistor is in bottom-gate configuration. (Note: Figure 6)

Re claim 16 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer comprises one or more units having high affinity for the first electrode. (Note: Figure 6)

Re claim 17 as applied to claim 15 above, Hirai teaches all the claimed limitations including, wherein the first electrode is surface treated prior to step (i) with a material containing one or more units having high affinity for the first electrode. (Note: Figure 6)

Re claim 20 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the transistor is a field-effect transistor. (Note: Figure 6)

Re claim 21 as applied to claim 1 above, Hirai teaches all the claimed limitations including wherein the transistor is a phototransistor. (Note: Figure 2)

Re claim 23, Hirai teaches a method of making an electronic or optoelectronic device comprising a transistor having first and second electrodes, a semiconductive layer, and a dielectric layer; said semiconductive layer comprising a semiconductive polymer and said dielectric layer comprising an insulating polymer; characterized in that said method comprises the steps of:

(i) depositing on the first electrode a layer of a solution containing material for forming the semiconductive layer and material for forming the dielectric layer; and

(Note: Column 15, lines 17-23)

(ii) optionally curing the layer deposited in step (i); (Note: Column 15, lines 30-36)

wherein, in step (i), the solvent drying time, the temperature of the first electrode and the weight ratio of (material for forming the dielectric layer): (material for forming the semiconductive layer) in the solution are selected so that the material for forming the semiconductive layer and the material for forming the dielectric layer phase separate by self-organisation to form an interface between the material for forming the semiconductive layer and the material for forming the dielectric layer. (Note: Column 15)

Re claim 24 and 25 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the electronic or optoelectronic device comprises an RF tag, electronic paper, chemical sensor, logic circuit, amplifier, or driver circuit. (Note: Figure 2)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2).

Re claim 3, as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the solvent drying time is in the range of from 0.1 to 100s. (Note: Column 19, lines 1-5)

In the case where the claimed ranges “overlap or lie inside ranges disclosed by the prior art” a prima facie case of obviousness exists. In *re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In *re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of “about 1-5%” while the claim was limited to “more than 5%.” The court held that “about 1-5%” allowed for concentrations slightly above 5% thus the ranges overlapped.); In *re Geisler*, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of “50 to 100 Angstroms” considered prima facie obvious in view of prior art reference teaching that “for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms].” The court stated that “by stating that suitable protection’ is provided if the protective layer is about’ 100 Angstroms thick, [the prior art reference] directly teaches the use of a thickness within [applicant’s] claimed range.”). Similarly, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. *Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (Court held as proper a rejection of a claim directed to an alloy of “having 0.8% nickel, 0.3% molybdenum, up to 0.1% iron, balance titanium” as obvious over a reference disclosing alloys of 0.75% nickel, 0.25% molybdenum, balance

titanium and 0.94% nickel, 0.31% molybdenum, balance titanium.). "[A] prior art reference that discloses a range encompassing a somewhat narrower claimed range is sufficient to establish a prima facie case of obviousness." In re Peterson, 315 F.3d 1325, 1330, 65 USPQ2d 1379, 1382-83 (Fed. Cir. 2003). >See also In re Harris, 409 F.3d 1339, 74 USPQ2d 1951 (Fed. Cir. 2005)(claimed alloy held obvious over prior art alloy that taught ranges of weight percentages overlapping, and in most instances completely compassing, claimed ranges; furthermore, narrower ranges taught by reference overlapped all but one range in claimed invention).< However, if the reference's disclosed range is so broad as to encompass a very large number of possible distinct compositions, this might present a situation analogous to the obviousness of a species when the prior art broadly discloses a genus. Id. See also In re Baird, 16 F.3d 380, 29 USPQ2d 1550 (Fed. Cir. 1994); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP § 2144.08.

Re claim 13 as applied to claim 11 above, Hirai teaches all the claimed limitations including, wherein the material for forming the dielectric layer has a surface tension in the range of from 15 to 35 dyn/cm. (Note: Column 4, lines 47-63)

In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of "about 1-5%" while the claim was limited to "more than 5%." The court held that "about 1-5%" allowed for concentrations slightly above 5% thus the ranges overlapped.); In re Geisler, 116 F.3d

1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of “50 to 100 Angstroms” considered prima facie obvious in view of prior art reference teaching that “for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms].”

Re claim 18 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the thickness of the dielectric layer is below 400nm. (Note: Column 9, line 32-34).

In the case where the claimed ranges “overlap or lie inside ranges disclosed by the prior art” a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990) (The prior art taught carbon monoxide concentrations of “about 1-5%” while the claim was limited to “more than 5%.” The court held that “about 1-5%” allowed for concentrations slightly above 5% thus the ranges overlapped.); In re Geisler, 116 F.3d 1465, 1469-71, 43 USPQ2d 1362, 1365-66 (Fed. Cir. 1997) (Claim reciting thickness of a protective layer as falling within a range of “50 to 100 Angstroms” considered prima facie obvious in view of prior art reference teaching that “for suitable protection, the thickness of the protective layer should be not less than about 10 nm [i.e., 100 Angstroms].”

Re claim 19 as applied to claim 1 above, Hirai teaches all the claimed limitations including, wherein the thickness of the semiconductive layer is in the range of 10 nm to 300nm. (Note: Figure 5 and 6)

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2) in view of Veres (US 7029945 B2).

Hirai teaches all the limitation of claim 1 in Paragraph 5 above.

However, Hirai does not explicitly disclose wherein the transistor is in top-gate configuration.

Veres teaches a process of manufacturing an organic field effect device is provided comprising the steps of (a) depositing from a solution an organic semiconductor layer; and (b) depositing from a solution a layer of low permittivity insulating material forming at least a part of a gate insulator, such that the low

permittivity insulating material is in contact with the organic semiconductor layer, wherein the low permittivity insulating material is of relative permittivity from 1.1 to below 3.0. In addition, an organic field effect device wherein the transistor is in top-gate configuration. N(Note: Figures 2c and 2d)

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to combine the invention of Veras with that of Hirai for sharp interface layers.

Correspondence

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip S. Green whose telephone number is 571-272-7024. The examiner can normally be reached on Monday thru Thursday 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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1/01/2008


BROOK KEBEDE
PRIMARY EXAMINER